REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claims 1 and 18 and have cancelled Claim 19. Specifically, Claim 1 has been amended to positively recite that the shared control gate *includes portions that lay above said floating gates*. Support for this amendment to Claim 1 is found throughout the specification of the present application including, for example, FIG. 1, in which the control (CG1) has portions that lay atop the floating gates, FG1 and FG2; Page 10, line 28-Page 11, line 3; and FIGS. 5-11 in which control gate 26 includes portions that lay atop the floating gates 18.

Insofar as Claim 18 is concerned, applicants have amended Claim 18 to include the features of Claim 1 as well as cancelled Claim 19. Further support for the amendment to claim 18 is found at Page 15, lines 7-15 of the specification of the instant application.

Since the above amendments to the claims do not introduce any new matter into the instant application, entry thereof is respectfully requested.

In the present Office Action, Claims 1-19 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 5,422,504 to Chang, et al. ("Chang, et al.") and U.S. Patent No. 5,658,816 to Rajeevakumar ("Rajeevakumar").

Applicants respectfully submit that the claims of the present application, as amended, are not obvious for the combined disclosures of Chang, et al. and Rajeevakumar since the applied references do not teach or suggest the features of the memory cells recited in Claims 1 and 18. Specifically, the disclosures of Chang, et al. and Rajeevakumar do not teach or suggest a pair of programmable memory cells including a control gate having portions thereof that overlay first and second floating gates having respective gate regions located on respective sides of the control gate. The inventive pair of programmable memory cells is illustrated in FIG. 1. As is illustrated, CG1 has portions that overlay FG1 and FG2.

Chang, et al. are defective since they do not teach or suggest applicants' claimed pair of programmable memory cells in which portions of the control gate lay atop the floating gates. In contrast thereto, Chang, et al. disclose an EEPROM memory array that includes a plurality of memory cells having a floating gate electrode 22 (See FIG. 1), 44 (See FIG. 5), 47,47' (See FIG. 9) and 74 (See FIG. 12) formed as sidewall spacers adjacent to a control gate electrode 20 (See FIG. 1), 30,32 (See FIG. 5), 30,32 (See FIG. 9) and 60,62 (See FIG. 12). As described and illustrated in the Chang, et al. disclosure, no portions of the control gate are located atop any portion of the floating gates. Hence, the claimed pair of programmable memory cells having the features recited in the claims of the present application is distinguishable and non-obvious from the EEPROM memory array disclosed in Chang, et al. Applicants find no motivation whatsoever in the disclosure of Chang, et al. which provides sufficient means for modifying the prior art memory cells to those presently claimed.

In the disclosure of Chang, et al., the control gate does not extend atop the floating gates therefore no portion thereof is located atop the floating gates, as is the case in the present claimed invention. Applicants' claimed configuration permits the control gate and the first and second floating gates to be located within a space of one lithographic square.

The applied secondary reference, i.e., Rajeevakumar, does not alleviate the above defects in Chang, et al. since Rajeevakumar does not teach or suggest applicants' claimed configuration of memory cells. Specifically, Rajeevakumar does not teach or suggest a pair of programmable memory cells including a control gate having portions thereof that overlay first and second floating gates having respective gate regions located on respective sides of the control gate. Rajeevakumar discloses a trench structure for a high density trench DRAM cell. Rajeevakumar does not mention the term "floating gate" any where in the disclosure, let alone that portions of the control gate lay atop floating gates that are located on respective sides of the control gate. As such, the disclosure of Rajeevakumar does not alleviate the defects in the disclosure of Chang, et al.

The § 103 rejection also fails because there is no motivation in the applied references which suggest modifying the disclosed structures to include the various features recited in the claims of the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. § 103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

Leslie S. Szivos, Ph.D.
Registration No. 39,394

Customer Number: 23389

LSS/sf